

# Producing research from undergraduate projects

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***Abstract:** Historically, undergraduate projects at AUT have centred on semi-commercial projects using standard engineering development techniques. Now, as the engineering school develops its research capability it has become possible to incorporate research objectives into undergraduate projects either as a partial or complete project. This paper presents four mechatronic/electronic projects whose primary purpose was to produce components that can be used for future research and discusses how they were introduced at the undergraduate level.*

## Introduction

Projects form a major part of AUT undergraduate engineering student assessment, beginning in Year two of the degree where the basics of project work are presented, continuing in year three with a semester length project and then cumulating in a year long project in the final year. The projects incorporate problem based learning, where skills in project planning, electronic design, printed circuit board (PCB) layout and mechanical construction are taught and assessed. The final year projects have historically been standard industrial projects where the primary focus has been the implementation of classical engineering techniques taught in previous classes to produce products for industry. We are now introducing a new range of student projects that create components that support the research activities of the school of engineering. These projects link with the research field being pursued by the supervisor, in this case evolutionary computation and evolvable hardware.

The main problem associated with undergraduate research projects is matching the level of the student to the level of the research. There are two approaches to minimizing this problem. The first is to select students pre-identified with the potential to undertake research projects. These students must be highly motivated and have a supervisor who can support them with specialised knowledge in areas outside the student's normal course requirements (e.g. tutoring in artificial neural networks or genetic algorithms). The second approach is for the supervisor to structure the project so that it can be undertaken by multiple groups, either working concurrently over one year or in separate stages over several years. For each student the supervisor sets specific goals which need to be completed by the end of the academic year. In order for this to be successful the supervisor must have a strong research focus, be able to view the project in a global perspective, be able to clearly identify the separate stages of the project and have realistic expectations of what undergraduate students can achieve.

At AUT we only select some of the students for undergraduate research projects; however other institutions make research projects mandatory at an undergraduate level (Olsson, Berndtsson, Lundell, & Hansson, 2003). The challenge of their approach is to enable students with less research capability to complete these projects. One way to manage this is introducing an integrated research components course where students have to complete a structured research proposal, a research paper, a poster and a presentation (Walker & Slotterbeck, 2006). For these less able students, the research component is simplified into a classically structured engineering problem.

Another method of including all students in a research-orientated final year project course is to format the projects in a similar fashion to a masters project, with the main difference being that the level of originality and significance is lower than a masters thesis (Olsson, Berndtsson, Lundell, & Hansson, 2003). This allows the projects to achieve the dual goals of preparing students for working life, and to test students for the potential to move into postgraduate research. In order to ensure students are meeting the research outcomes the students have timelines with fixed deadlines or assessment points, which prevents them from moving into research dead ends.

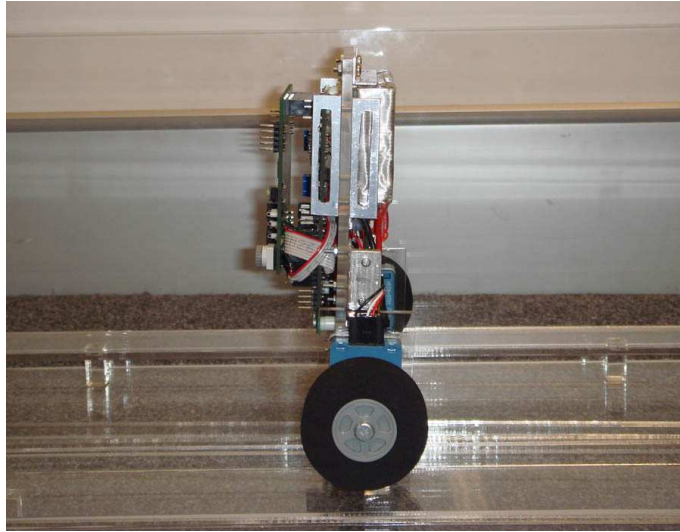
Additionally, undergraduate research can be managed by utilising research groups comprised of both undergraduate and postgraduate students (Bernat, Teller, Gates, & Delgado, 2000). These research groups are arranged in a non-hierarchical model. Larger research groups may consist of small research groups with a mixture of undergraduate and postgraduate students. This allows undergraduate students to learn the research process from postgraduate students and relate the research to the industrial world.

The combination of research and undergraduate projects is not new, and several universities have had success with their implementations (Koeller, 2005). Some of the benefits of undergraduate research are: the increased ability to select and motivate students for postgraduate studies with an associated increase in the number of students entering postgraduate studies (Narayanan, 1999), an increase in the number of students having a deep comprehension of their subject, the value of products generated by the university is increased, the introduction of state of the art technologies to the university at core levels (Ghafoori & Honaker, 1999), and finally lecturers can combine the goals of academic instruction and primary research with an increased industrial co-operation (Dessouky, Magdy, Mahmoud, Aly, & Soliman, 2004).

This paper discusses how projects that can be used for future research was introduced to undergraduate projects using four projects as examples; virtual FPGA architectures, evolvable mobile inverted pendulum, evolvable balancing beam, and a Khepera interface board.

## Projects

### Mobile Inverted Pendulum



**Figure 1: Mobile Inverted Pendulum in its tank**

The research goal for this project was to create a mobile inverted pendulum (MIP) controller using evolutionary computation. Research was previously performed by the authors and several papers produced with the concept in simulation (Beckerleg & Collins, 2006, 2007). This project required a much higher level of engineering and understanding than is expected from a normal undergraduate project. To make the project achievable it was broken into manageable stages.

The first stage was to create a MIP using standard engineering techniques. This was performed by two teams of highly ranked third year students who successfully created the chassis, circuit design and software for the first MIP using a standard PID controller. The software and hardware design was complex including the use of gyroscopes, accelerometers and Kalman filters. An external H-bridge motor control was purchased to reduce the requirements of the project. The pendulum was able to balance with the added ability of being remotely controlled.

The second stage was a redesign of the electronics and chassis with the aim of creating a small generic board that could be incorporated into any chassis design. The H-bridge motor control, gyroscopes and accelerometers were brought onto the one board. The design required the pendulum to balance using its own processor or to be controlled by various AUT daughter boards. These daughter boards have a range of different processors and FPGAs allowing different methods of control to be used and evaluated. A second generation chassis, circuits and PCB were designed and built and the pendulum made to balance using a standard PID controller.

The third stage was to create the MIP controller using an evolutionary process. This required the creation of additional circuitry, boards and chassis. In order for the pendulum to evolve, it would need to repeatedly evaluate individual chromosomes without human intervention. In order to achieve this, the motion of the pendulum was limited by placing it in a tank with rails. The pendulum would begin the test by centering itself in the tank, and downloading the new chromosome to be tested from a PC. It would then see how well the chromosome would maintain balance, feeding the distance traveled and pendulum tilt back to the PC. When the test was completed the pendulum would automatically re-center and await the next chromosome. The new chassis, circuitry and tank have been built and we are in the final stages of testing.

The final stage is currently being undertaken where the simulated results are tested against the actual pendulum.

## Balancing Beam



**Figure 2 Balancing Beam**

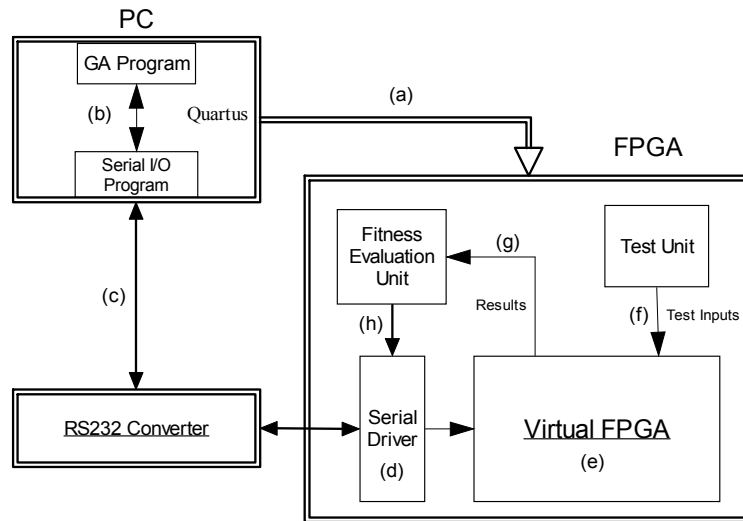
The research goal for this project was to compare four different methods of control for an unstable balancing beam. The four methods under investigation were PID control, fuzzy logic, artificial neural networks (ANN) and evolutionary computation. The aim of the controller was to stabilize the ball at the centre of the beam in the shortest time. This project was an expansion of existing flat beams that are supplied for normal control experiments; in this case the beam was a convex curve with a high curvature rate making it extremely difficult to maintain balance and stability. The project was made even harder by the fact that the motor has a limited speed which prevents the beam from reacting swiftly to changes in the ball position. Once again the project was broken down into sections and implemented by groups of students over several years.

The first stage was to perform the initial research, design conception, circuit design and mechanical construction of the beam. A large part of the first stage was taken up in the mechanical construction of the bridge, in particular the mounting of the stepper motor and gear box assembly, the beam and the convex curve. The beam was handcrafted by the student using both standard engineering manufacture for the base and a 3D printer for the convex curve. To detect the ball position twenty one modulated infra-red sensors used were mounted on the beam. The control circuits and PCB were also designed in this stage.

The second stage was to test the characteristics of the beam and to improve on the original design. The circuits were heavily modified to improve the performance of the beam, a LCD display and driver added, the stepper motor drivers were increased in power, and an extra 1 megabyte of memory added to the microcontroller via the SPI port. This memory was required so that intrinsic evolution can be performed, with the memory used to store a population of one hundred chromosomes. At this stage the beam was to balance the ball using both a PID and a fuzzy logic controller.

The third stage, yet to be completed, involves a computer simulation of the beam where a controller can initially be evolved using genetic programming. This will require the mathematical modeling of the beam, and the creation of a genetic algorithm. Once complete, the evolutionary process will be transferred to the physical beam itself with the genetic process occurring intrinsically. In a separate stage, an ANN will be created and trained to balance the ball. When concluded, the four different controllers can then be compared and the long term research objectives of this project completed.

## Virtual FPGA



**Figure 3: Block diagram of extrinsic evolution of a virtual FPGA.**

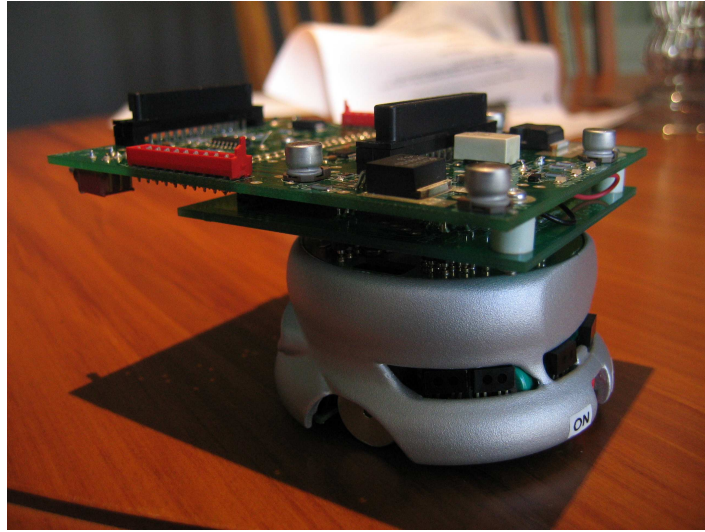
The research goal for this project was to evolve hardware for circuit design, initially replicating Thompson's classic experiment on evolutionary hardware (Thompson, 1997), and then moving towards evolvable hardware in robotic controllers. This is an ongoing research project that investigates the creation of a virtual FPGA which overcomes the inherent problems of a real world FPGA with regard to evolvable structures. The scope of the project was broken into parts that were partitioned into projects spread over several years.

In the first stage the students investigated the creation of virtual FPGA architectures and how they could be synthesised in a FPGA. The hardware used was the "Altera UP2 Education Board" containing the FLEX FPGA. The students created a program on the computer which enabled a configuration bit stream to be downloaded to the virtual FPGA via a VHDL created serial interface. The virtual FPGA created was based on the S-block (Haddow & Tufte, 2000), which has the added ability to use its configurable logic blocks as part of the FPGA routing. The S-block was tested and confirmed to be operating as intended.

The second stage was the creation of an adaptor board that would allow the more powerful AUT daughter board with the Cyclone II FPGA to be used. Also a virtual FPGA was made that mimics the Xilinx XC6216 series FPGA that was used by Thompson. This architecture was again verified by downloading test configuration bit streams.

The third stage was to evolve a tone generator using the Xilinx series virtual FPGA year and then to create FPGA architectures that are more suited to this experiment than the original architecture used by Thompson.

## Khepera interface



**Figure 4: Khepera Interface board**

The research goal for this project was to evolve hardware to control the motion of a Khepera II robot. The Khepera robot has become a standardized platform for robotic research, used in universities around the world. The robot is small in size and has an expansion bus that allows adaptor boards to be added to the robot via a turret system. Evolvable hardware research has been used on this robot via a commercially available expansion turret containing a Xilinx XC6216 FPGA. However this FPGA is now out of date. AUT have a range of controller boards with using processors including the 8 bit ATMEL AVR series, the 32 bit ARM processor and the powerful Cyclone II FPGA. Research in evolvable hardware could be advanced if the AUT controller boards could be interfaced to the Khepera robot.

The first stage of the project was to create an interface board that could connect the expansion bus of the Khepera to the control systems of the AUT boards, and also to hold a rechargeable battery so that the Khepera's own power system would not be additionally loaded. The board created presented a number of technically difficult problems, the rechargeable battery used was a lithium battery that has a danger of explosion if incorrectly charged, the voltage levels of the Khepera and AUT boards are different, thus requiring voltage translation and the size of the board had to be as kept to a minimum, which required the creation of a double sided PCB. The design, construction and implementation was successfully performed by the student.

The second stage of the project was to use the AUT boards to control the robot and perform tasks such as obstacle avoidance. The Khepera itself contains a 32 bit Motorola micro-controller which has an onboard BIOS system. The BIOS can be accessed via a serial interface made available at the expansion ports. The BIOS allows independent monitoring and control of the robot, where all the onboard sensors can be read, and the motor direction and speed controlled. This control of the Khepera was initially performed with the ATMEL AVR, and then controlled by a NIOS 32 processor configured on the AUT FPGA board. This required the students to investigate the use of the NIOS processor, previously unused in our department. This was successfully completed by two students and the knowledge gained has been passed on to corresponding courses.

The third stage of the project, yet to be completed is to create evolvable hardware modules that can be used to control the motion of the robot.

## Conclusions

It has been demonstrated that projects to be used for future research can be performed by undergraduate students. This is achieved by: matching the student's level and abilities to the project, dividing the project into stages that can extend over several years with each stage of the project being assessable, and giving the students specialist training in fields outside their normal expertise. The advantages these projects bring are: increased knowledge and state of the art technologies, the ability to select and motivate students for postgraduate studies, and an expansion of the lecturers own research outputs.

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